HN

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/061,671	02/01/2002	Michael A. Filippo	5500-68500	9586

7590 05/17/2005

Robert C. Kowert
Conley, Rose, & Tayon, P.C.
P.O. Box 398
Austin, TX 78767

EXAMINER	
WANG, ALBERT C	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/061,671	FILIPPO, MICHAEL A.	
	Examiner	Art Unit	
	Albert Wang	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/3/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is responsive to the amendment filed March 3, 2005. The provisional double patenting rejection is reiterated, as it has not been addressed. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-16 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-16 of copending Application No. 10/061,792. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims of copending Application are worded nearly identically with those of the instant Application, with the exception that the copending Application uses clock control, whereas the instant Application uses clock control. Clock control is an obvious means of clock control.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-8 and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gunther et al., U.S. Patent No. 5,781,783 ("Gunther"), in view of Bartley, U.S. Patent No. 6,219,796.

As per claim 1, Gunther teaches an integrated device (figs. 1 & 2, processor 14), comprising:

a plurality of functional units, wherein each functional unit is configured to receive one or more input signals, perform an operation or task, and produce one or more output signals (fig. 2, circuit blocks 32-56), wherein each functional unit configured to be inactive while one or more of the other functional units is active (col. 5, lines 47-61);

a plurality of activity detector and clock control units coupled to said plurality of functional units (figs. 3 & 4, clock control circuits 60 & 84; col. 12, lines 4-16), wherein each activity detector and clock control unit is associated with a different one of the functional units and configured to predict when its associated functional unit will be inactive (col. 5, lines 29-39; col. 12, lines 4-10).

wherein each activity detector and clock control unit is configured to switch off a clock to its associated functional unit in response to its associated functional unit being predicted inactive

and provide the clock to its associated functional unit when its associated functional unit is active (col. 5, lines 47-61; col. 10, line 62 – col. 11, line 8).

However, Gunther does not expressly teach that a functional unit is predicted to be inactive for at least a threshold amount of time before shutting off its clock. Bartley teaches such a threshold amount of time (col. 7, lines 11-21, "clock down threshold"). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Bartley's use of a clock down threshold to Gunther's integrated device. A motivation for doing would have been to avoid inefficient cycling between on and off states (Bartley, col. 7, lines 11-21).

As per claim 2, Gunther teaches a first one of the activity detector and clock control units is configured to monitor a number of events which correspond to input and output signals for a first one of the functional units (col. 9, line 55 – col. 10, line 10).

As per claims 3, Gunther teaches the input signals received by the first functional unit comprise control signals for controlling the operation of the first functional unit, and wherein the first activity detector and clock control unit is configured to monitor one or more of the control signals to predict when the first functional unit will be inactive (col. 6, lines 29-54; col. 12, lines 4-16).

As per claim 4, Gunther teaches the input signals received by the first functional unit comprise data operated on by the first functional unit, and wherein the first activity detector and clock control unit is configured to monitor the flow of data to the first functional unit to predict when the first functional unit will be inactive (col. 6, lines 29-54; col. 12, lines 4-16).

As per claim 5, Gunther teaches the input signals received by the first functional unit comprise instructions to be performed by the first functional unit, and wherein the first activity

detector and clock control unit is configured to monitor the instruction flow to the first functional unit to predict when the first functional unit will be inactive (fig. 5; col. 4, lines 34-46).

As per claim 6, Gunther teaches a first one of the activity detector and clock control units is further configured to determine if its associated functional unit has been inactive (col. 5, lines 29-39). Bartley teaches applying a threshold amount of time (col. 7, lines 11-21).

As per claim 7, Bartley teaches the clock down threshold may be for different functional units and for different modeling techniques (col. 7, lines 11-21), implying that the threshold is programmable. Gunther teaches a programmable register for holding a threshold value (col. 9, lines 39-41).

As per claim 8, Gunther teaches each of the activity detector and clock control units comprises:

an activity detector configured to determine when the associated functional unit is inactive ((figs. 3 & 4, clock control circuits 60 & 84; col. 12, lines 4-16)); and

a clock gate coupled to the activity detector and configured to receive a main clock source for the integrated device and provide a functional unit clock source to the associated functional unit (fig. 3, gate 74; col. 10, line 62 – col. 11, line 8);

wherein the activity detector is configured to control the clock gate to shut off the functional unit clock source for the associated functional unit when the associated functional unit is inactive (col. 5, lines 47-61).

As per claim 10, Gunther teaches a microprocessor (figs. 1 & 2, processor 14), comprising:

an integer execution unit configured to receive an integer instruction stream and execute integer instructions from the integer instruction stream (fig. 2, integer execution unit 48);

a floating point execution unit configured to receive a floating point instruction stream and execute floating point instructions from the floating point instruction stream (fig. 2, floating point unit 50);

an integer activity detector unit coupled to the integer instruction stream and configured to predict when the first functional unit will be inactive and shut a clock off to the integer execution unit when it is inactive (figs. 3 & 4, clock control circuits 60 & 84 corresponding to BIU and cache memory; col. 12, lines 4-16, applicable to integer execution unit; col. 5, lines 29-39 & 47-61; col. 10, line 62 – col. 11, line 8); and

a floating point activity detector unit coupled to the floating point instruction stream and configured to predict when the floating point execution unit will be inactive and shut clock off to the floating point execution unit when it is inactive (figs. 3 & 4, clock control circuits 60 & 84 corresponding to BIU and cache memory; col. 12, lines 4-16, applicable to floating point unit; col. 5, lines 29-39 & 47-61; col. 10, line 62 – col. 11, line 8).

However, Gunther does not expressly teach that integer execution unit is predicted to be inactive for at least a threshold amount of time before shutting off its clock. Bartley teaches a threshold amount of time when no instructions will be presented (col. 7, lines 11-21, "clock down threshold"). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Bartley's use of a clock down threshold to Gunther's integer execution unit. A motivation for doing would have been to avoid inefficient cycling between on and off states (Bartley, col. 7, lines 11-21).

As per claim 11, Gunther does not expressly teach that floating point execution unit is predicted to be inactive for at least a threshold amount of time before shutting off its clock. Bartley teaches a threshold amount of time when no instructions will be presented (col. 7, lines 11-21, "clock down threshold"). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Bartley's use of a clock down threshold to Gunther's floating point execution unit.

As per claim 12, Bartley teaches the clock down threshold may be for different functional units and for different modeling techniques (col. 7, lines 11-21), implying that the threshold is programmable. Gunther teaches a programmable register for holding a threshold value (col. 9, lines 39-41).

4. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gunther/Bartley as applied to claim 1 above, and further in view of Pappert, U.S. Patent No. 6,380,760.

As per claim 9, Gunther/Bartley does not expressly teach an output emulator configured to drive the output signals for a first one of the functional units to a safe state when clock is shut off to the first functional unit. Pappert teaches an output emulator to drive output signals to a tri-stated, or high impedance state, when clock is shut off to a first functional unit (fig. 1, contention detection circuit 12; col. 2, lines 50-59; col. 3, lines 14-21). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Pappert's output emulator to Gunther/Bartley's integrated device, as a way to prevent buffer contention (Pappert, col. 1, lines 25-44).

5. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gunther et al., U.S. Patent No. 5,781,783 ("Gunther"), in view of Suzuki, U.S. Patent No. 5987,616.

As per claim 13, Gunther teaches a microprocessor (figs. 1 & 2, processor 14), comprising:

an instruction fetch and decode unit configured to fetch and decode microprocessor instructions (fig. 2, prefetcher 34 and decoder 42);

an instruction scheduler configured to receive an instruction stream from the instruction fetch and decode unit (fig. 2, control unit 46), wherein the instruction scheduler is further configured to buffer the instruction stream and schedule instructions from the instruction stream for execution (col. 6, lines 40-46);

an integer execution unit configured to receive integer instructions from the instruction scheduler and execute the integer instructions (fig. 2, integer execution unit 48);

a floating point execution unit configured to receive floating point instructions from the instruction scheduler and execute the floating point instructions (fig. 2, floating point unit 50);

an activity detector coupled to the instruction scheduler and configured to monitor the instruction stream to predict a lack of instructions for another functional unit (figs. 3 & 4, clock control circuits 60 & 84 corresponding to BIU and cache memory; col. 12, lines 4-16, applicable any circuit block; col. 10, lines 23-40, monitor circuit block A to predict when to clock down circuit block C).

However, though Gunther gives examples of an activity detector predicting inactivity of a single functional unit, Gunther does not expressly teach a combined activity detector to predict a lack of instructions for both the integer execution unit and the floating point execution unit.

Suzuki teaches coupling an activity detector to any one of a plurality of units (figs. 1-4, PMUs 3-3c are coupled to different units). Suzuki's activity detector predicts a lack of instructions for both the integer execution unit and the floating point execution unit (figs. 1-4, for both integer operation part 8 and floating point part 9; col. 5, lines 9-21). At the time of the invention, it would have been obvious to one of ordinary skill in the art to coupled Suzuki's combined activity detector to Gunther's instruction scheduler, as combining separate activity detectors into a single activity detector is a matter of design, especially if the separate activity detectors were monitoring the same instruction scheduler.

Suzuki also teaches:

a first power control unit configured to control power to the integer execution unit (figs. 1-4, leak cut switch 6), wherein said first power control unit is configured to shut off power to the integer execution unit in response to the activity detector predicting a lack of integer instructions in the instruction stream (col. 5, lines 9-21); and

a second power control unit configured to control clock to the floating point execution unit (figs. 1-4, leak cut switch 7), wherein said second power control unit is configured to shut off power to the floating point execution unit in response to the activity detector predicting a lack of floating point instructions in the instruction stream (col. 5, lines 9-21).

Gunther teaches interchanging power control with clock control (col. 10, line 62 – col. 11, line 8).

6. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gunther/Suzuki, as applied to claim 13 above, and further in view of Bartley, U.S. Patent No. 6,219,796.

As per claim, Gunther/Suzuki does not expressly teach that the floating point unit is predicted to be inactive for at least a threshold amount of time before shutting off its clock. Bartley teaches a threshold amount of time when no instructions will be presented (col. 7, lines 11-21, "clock down threshold"). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Bartley's use of a clock down threshold to Gunther/Suzuki's integrated device. A motivation for doing would have been to avoid inefficient cycling between on and off states (Bartley, col. 7, lines 11-21).

As per claim 15, Suzuki teaches the activity detector is configured to monitor the instruction stream to detect the presence of floating point instructions in the instruction stream and control the second power control unit to restore clock to the floating point execution unit when a floating point instruction is scheduled for the floating point execution unit (col. 5, lines 9-21). Gunther teaches interchanging power control with clock control (col. 10, line 62 – col. 11, line 8).

7. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gunther et al., U.S. Patent No. 5,781,783 ("Gunther"), in view of Suzuki, U.S. Patent No. 5987,616, and Bartley, U.S. Patent No. 6,219,796.

As per claim 16, Gunther teaches an integrated device (figs. 1 & 2, processor 14), comprising:

a first functional unit configured to receive an first input and perform a first operation or task according to the first input (fig. 2, a first of circuit blocks 32-56);

a second functional unit configured to receive a second input and perform a second operation or task according to the second input (fig. 2, a second of circuit blocks 32-56);

activity detectors coupled to the first and second inputs and configured to determine when the first function unit will be inactive and when the second functional unit will be inactive (figs. 3 & 4, clock control circuits 60 & 84 corresponding to BIU and cache memory; col. 12, lines 4-16, applicable any circuit block; col. 10, lines 23-40);

However, though Gunther gives examples of an activity detector predicting inactivity of a single functional unit, Gunther does not expressly teach a combined activity detector to predict a lack of instructions for both the integer execution unit and the floating point execution unit. Suzuki teaches coupling an activity detector to any one of a plurality of units (figs. 1-4, PMUs 3-3c are coupled to different units). Suzuki's activity detector predicts a lack of instructions for both the integer execution unit and the floating point execution unit (figs. 1-4, for both integer operation part 8 and floating point part 9; col. 5, lines 9-21). At the time of the invention, it would have been obvious to one of ordinary skill in the art to coupled Suzuki's combined activity detector to Gunther's instruction scheduler, as combining separate activity detectors into a single activity detector is a matter of design, especially if the separate activity detectors were monitoring the same third functional unit.

Suzuki also teaches:

a first power control unit configured to control power to the integer execution unit (figs. 1-4, leak cut switch 6), wherein said first power control unit is configured to shut off power to

the integer execution unit in response to the activity detector predicting a lack of integer instructions in the instruction stream (col. 5, lines 9-21); and

a second power control unit configured to control clock to the floating point execution unit (figs. 1-4, leak cut switch 7), wherein said second power control unit is configured to shut off power to the floating point execution unit in response to the activity detector predicting a lack of floating point instructions in the instruction stream (col. 5, lines 9-21).
Gunther teaches interchanging power control with clock control (col. 10, line 62 – col. 11, line 8).

Lastly, Gunther does not expressly teach that a functional unit is predicted to be inactive for at least a threshold amount of time before shutting off its clock. Bartley teaches such a threshold amount of time (col. 7, lines 11-21, "clock down threshold"). At the time of the invention, it would have been obvious to one of ordinary skill in the art to apply Bartley's use of a clock down threshold to Gunther/Suzuki's integrated device. A motivation for doing would have been to avoid inefficient cycling between on and off states (Bartley, col. 7, lines 11-21).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert Wang whose telephone number is 571-272-3669. The examiner can normally be reached on M-F (9:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

aw
May 11, 2005

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100